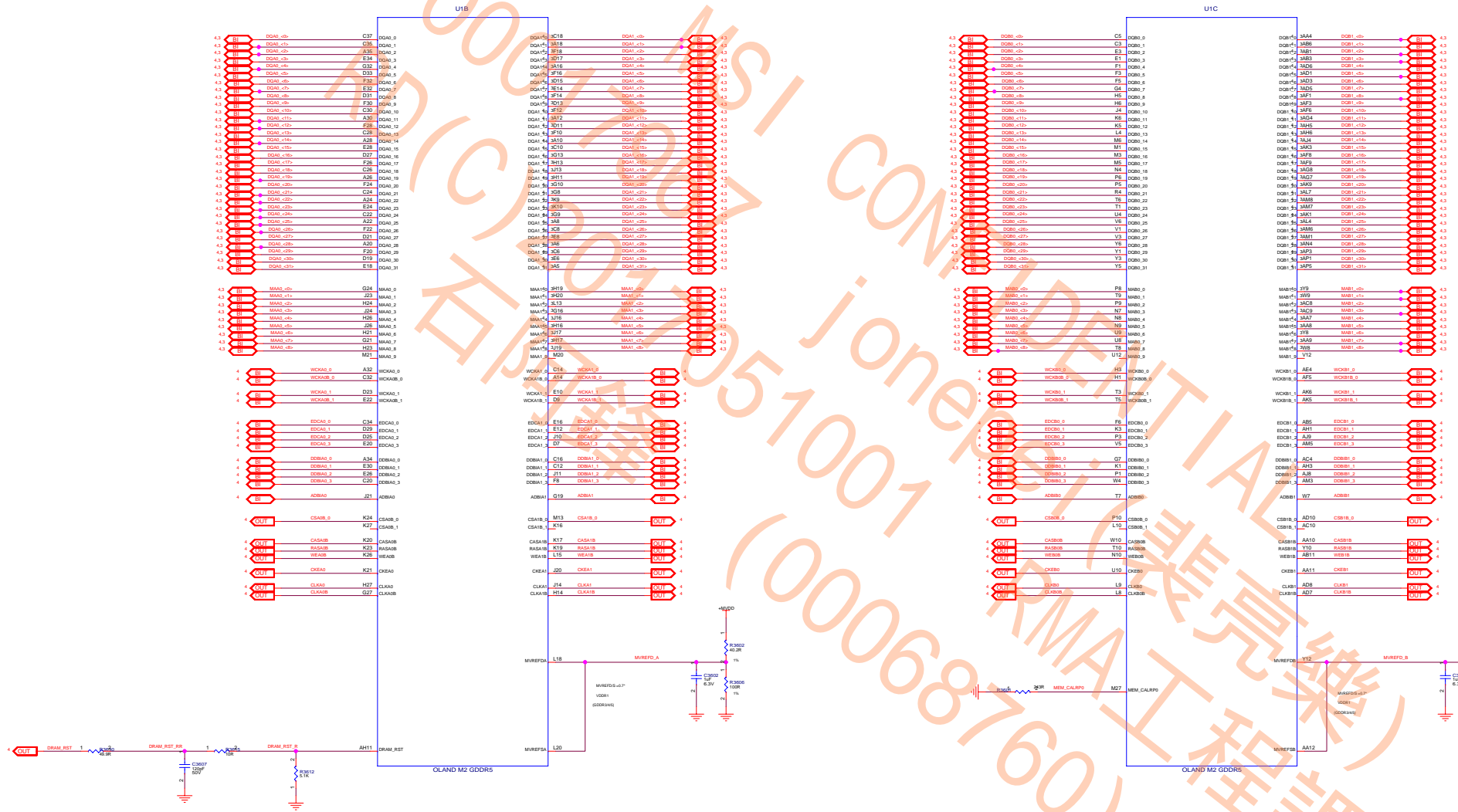


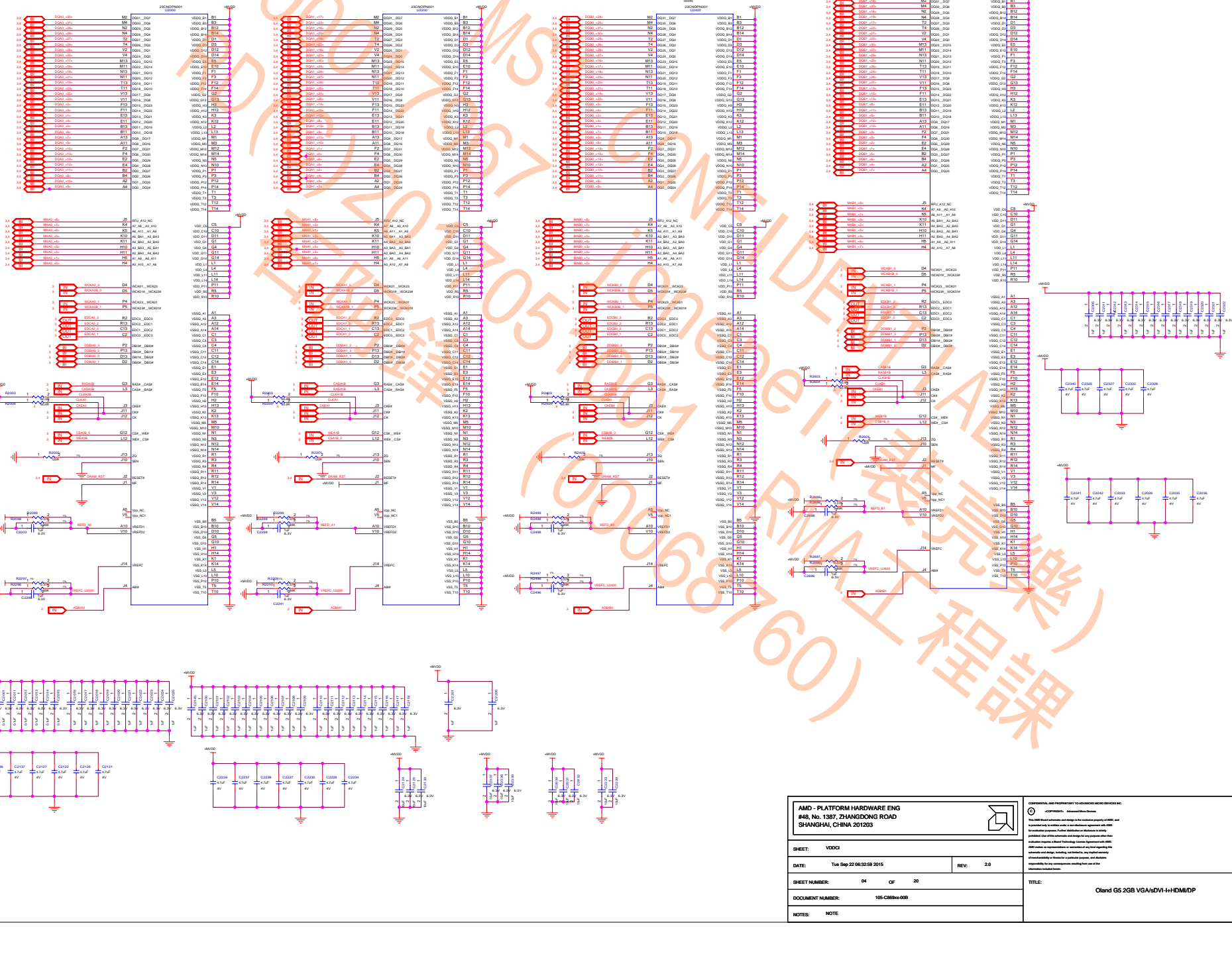
REV: 2.0

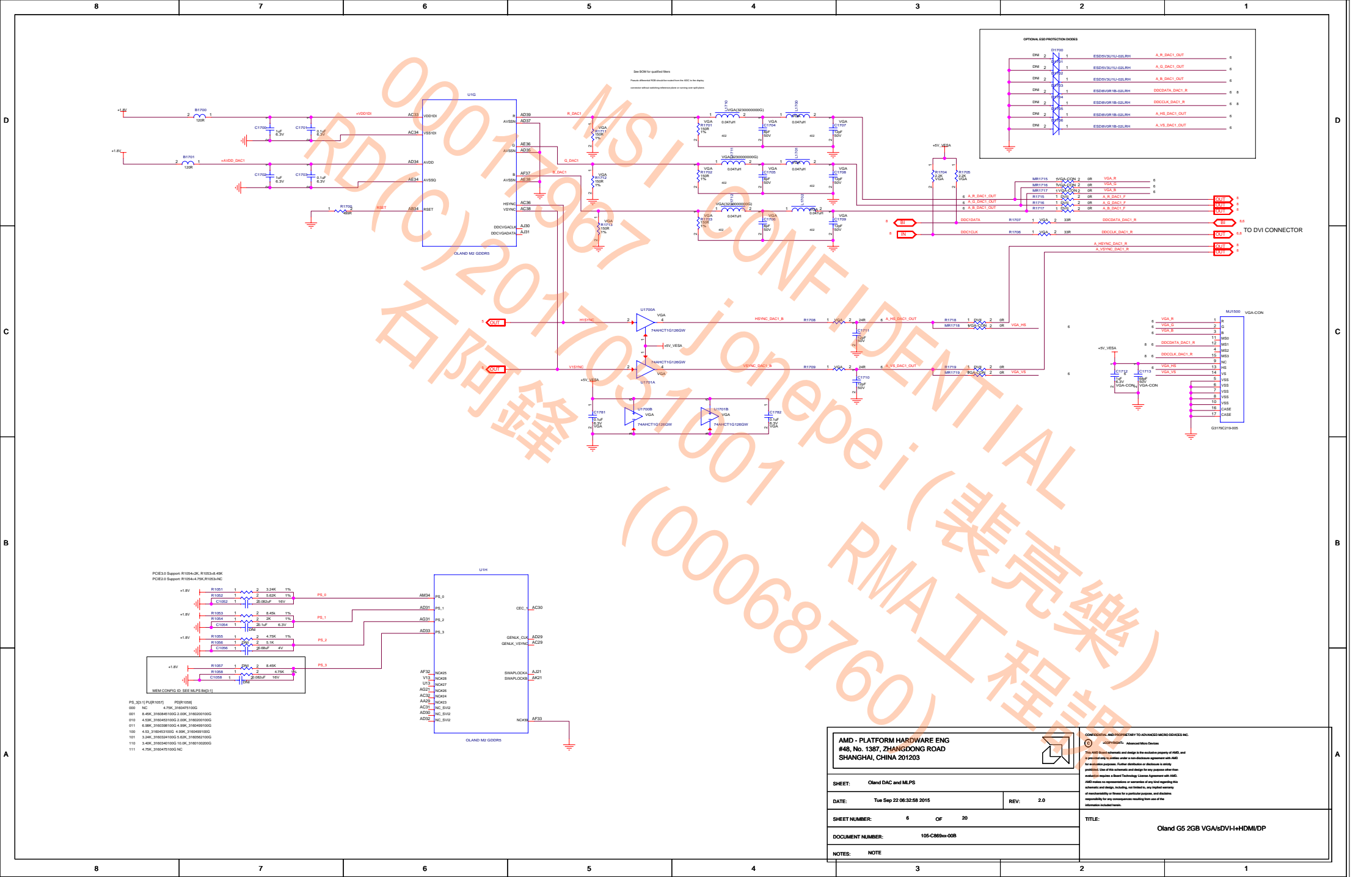
REV: 2.0

TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

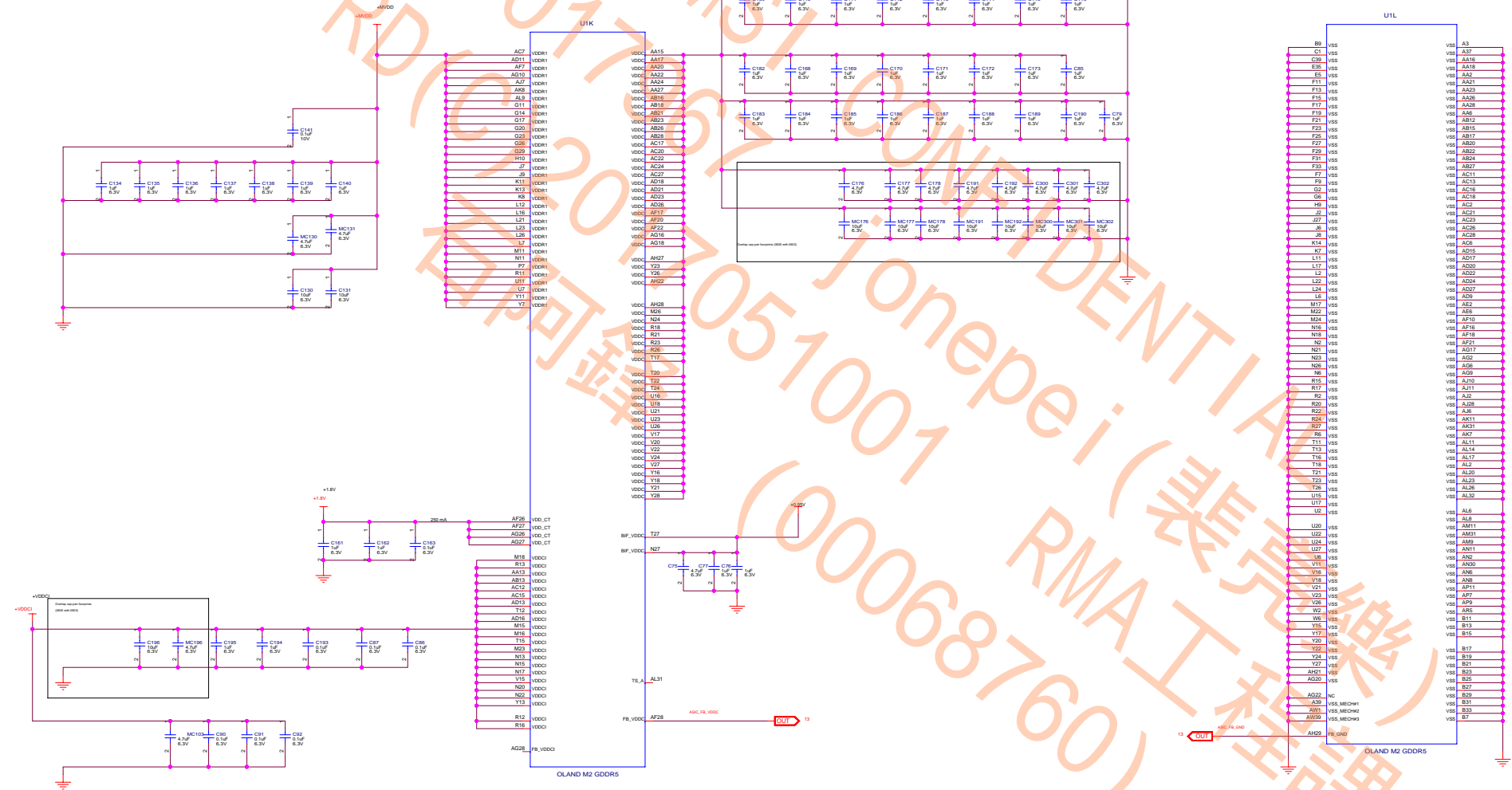
Grand CC 200 10/10/2011 11:12:00 AM







OLAND Power & GND



AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203



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SHEET: Oland Power&GND

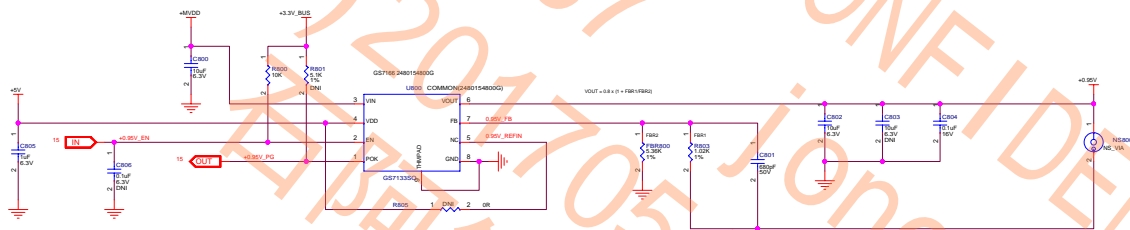
DATE: Mon Sep 21 10:05:46 2015

REV: 2.0

SHEET NUMBER: 9 OF 20

TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

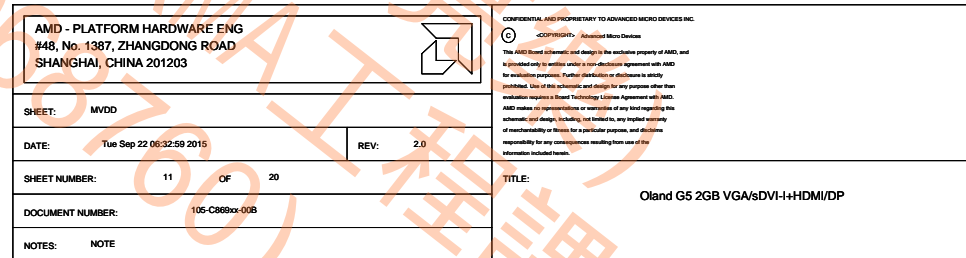
LDO #1:	$V_{in} = +1.5V \pm 2\%$	$V_{out} = +0.95V \pm 2\%$	$I_{out} = 1.44A$ (TYP) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			

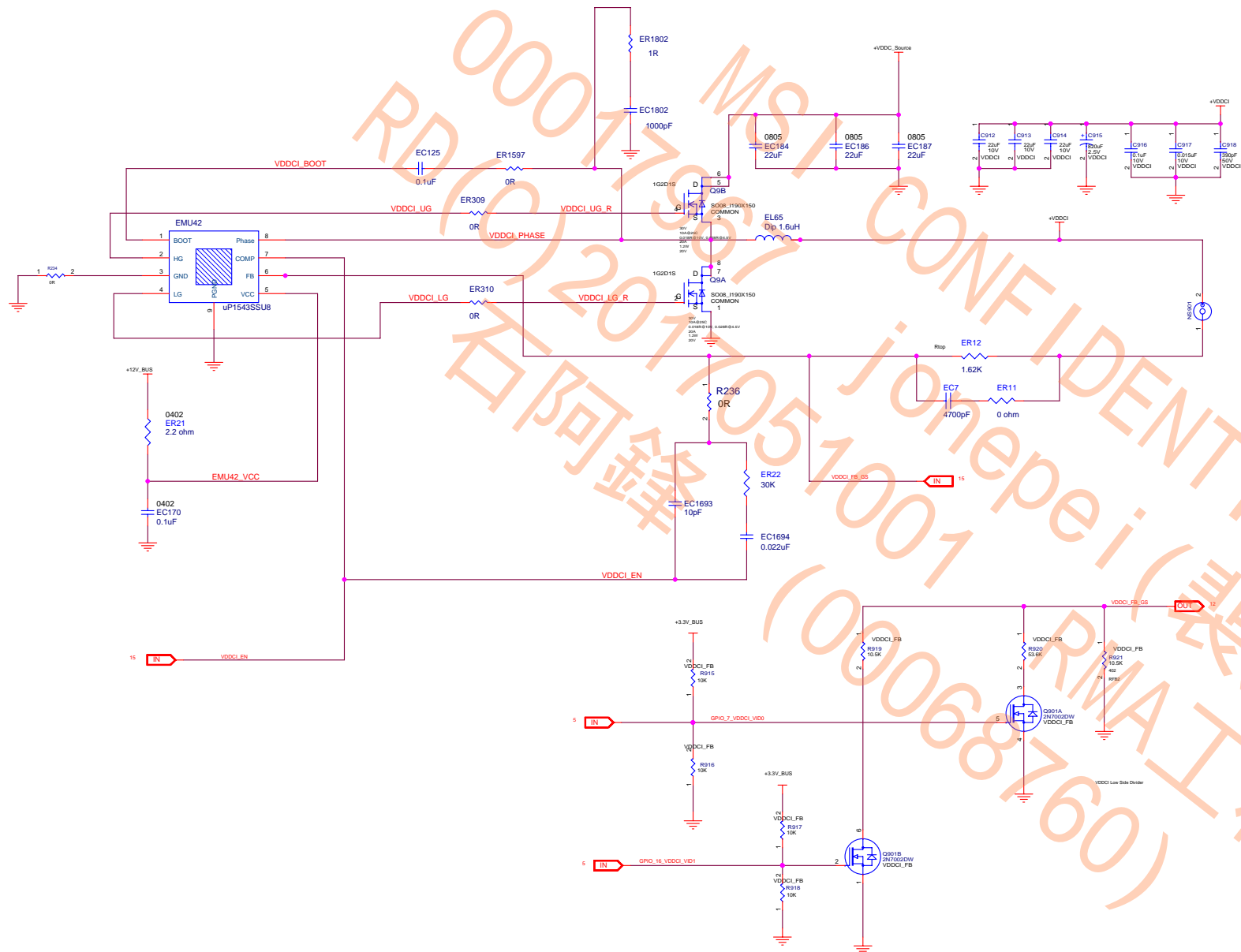


REV: 2.0

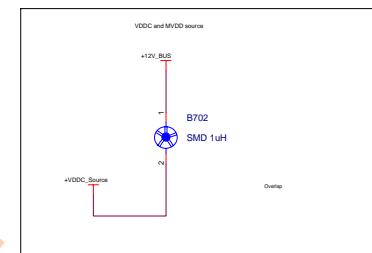
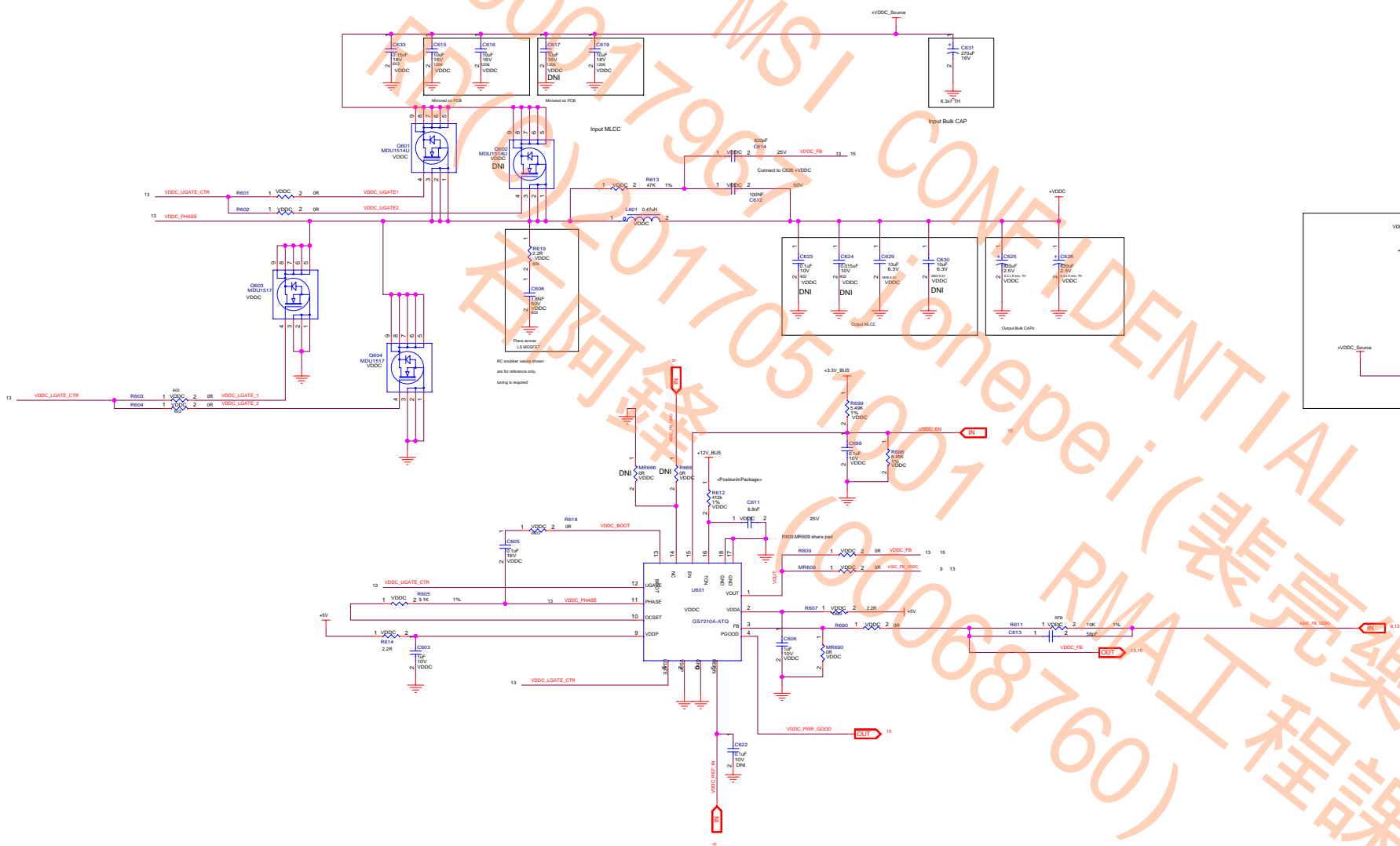
TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

DOCUMENT NUMBER: 105-C869xx-00B





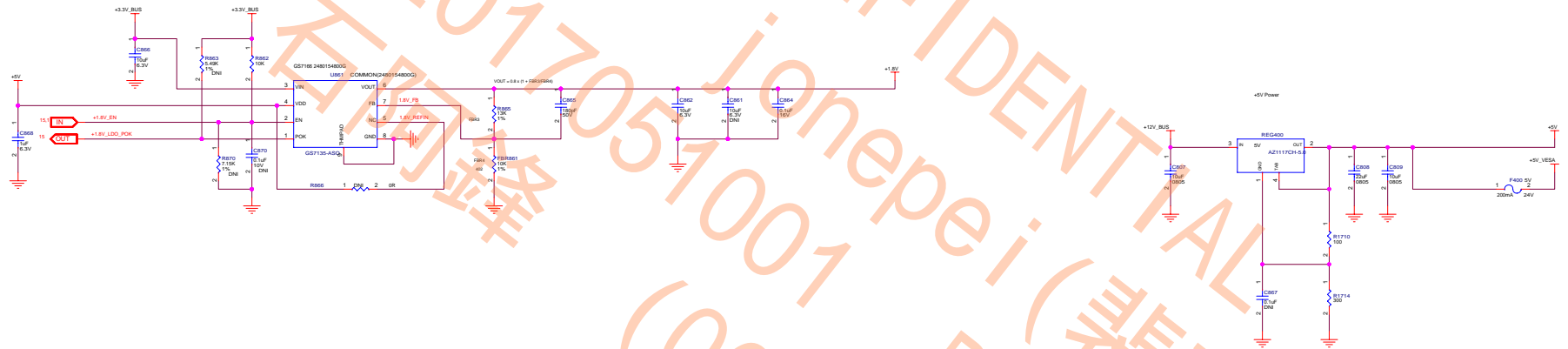
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SHEET: VDDCI			TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP		
DATE: Tue Sep 22 06:32:59 2015		REV: 2.0			
SHEET NUMBER: 12 OF 20					
DOCUMENT NUMBER: 105-C869xx-00B					
NOTES: NOTE					



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SHEET: VDDC		TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP	
DATE: Tue Sep 22 06:32:59 2015		REV: 2.0	
SHEET NUMBER: 13 OF 20			
DOCUMENT NUMBER: 105-C880x-008			
NOTES: NOTE			

Linear Regulators

LDO I2: $V_{in} = 3.00V$ to $3.60V$ (3.3V \pm 9%) $V_{out} = +1.8V$ \pm 2% $I_{out} = 1.6A$ (TbV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



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SHANGHAI, CHINA 201203

SHEET: VDDCI

DATE: Tue Sep 22 06:32:59 2015

SHEET NUMBER: 14 OF 20

DOCUMENT NUMBER: 105-C869xx-008

NOTES:	NOTE
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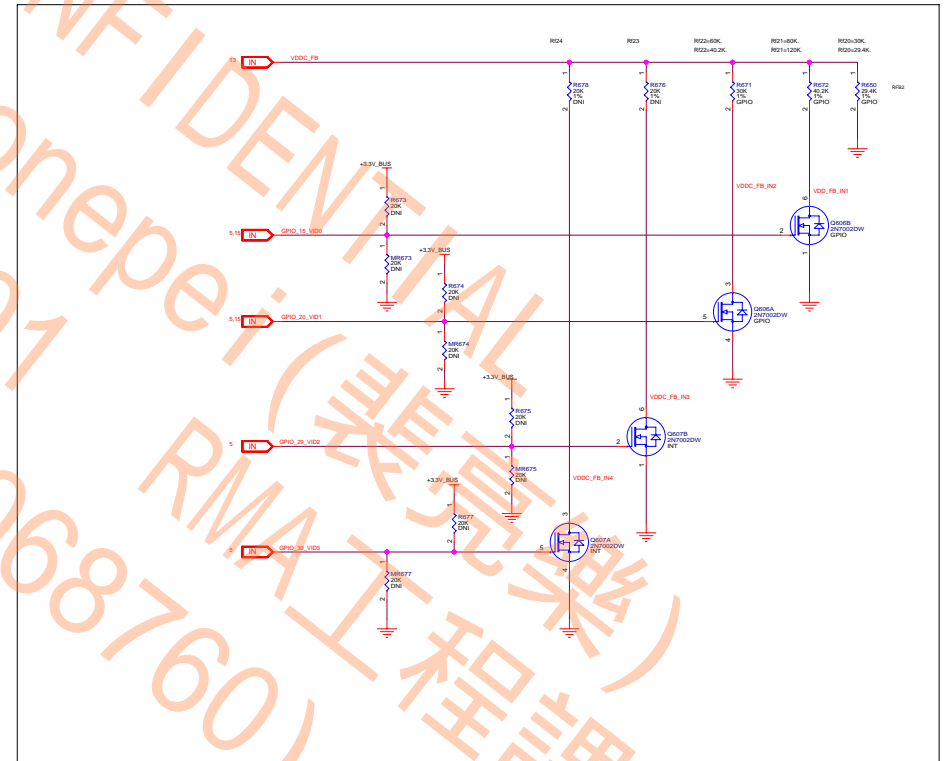
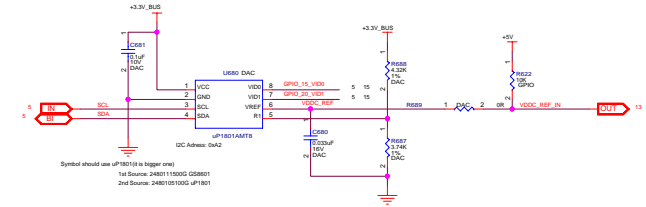
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TITLE:

Oland G5 2GB VGA/sDVI-I+HDMI/DP

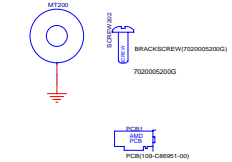
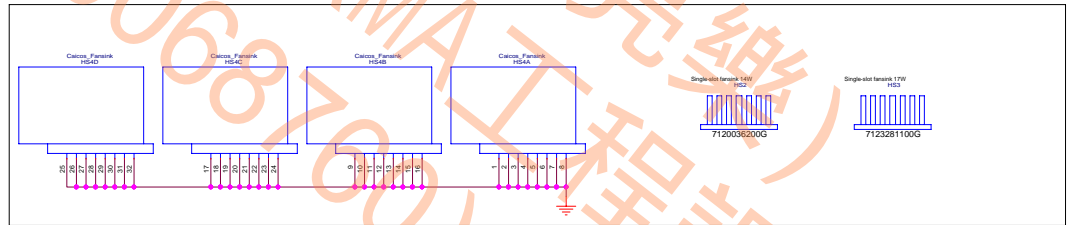
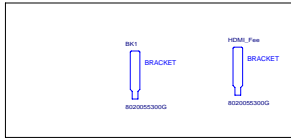
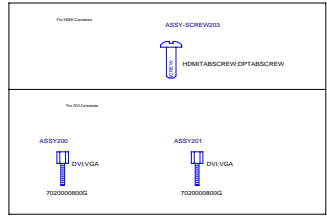
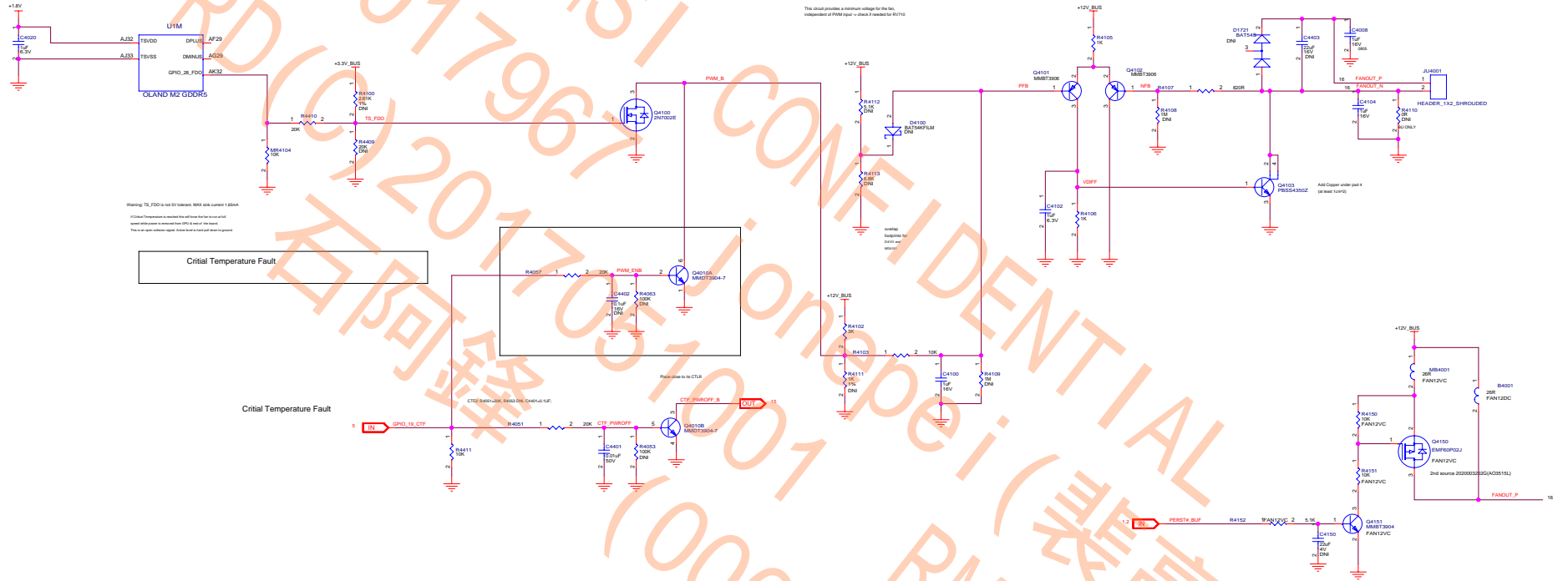


SHEET: VDDC	
DATE: Tue Sep 22 06:32:59 2015	REV: 2.0
SHEET NUMBER: 15 OF 20	
DOCUMENT NUMBER: 105-C869xx-00B	
NOTES: NOTE	

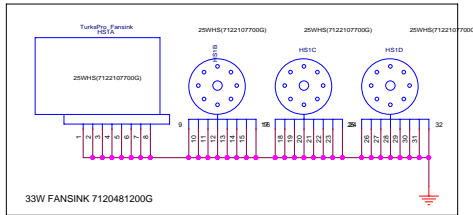
TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

Mechanical and Thermal Management

Install R4023	GPIO6 is 0: Fan stop GPIO6 is PWM: Fan running
Install R40116 Q4011, R40119	GPIO6 is 0: Fan stop GPIO6 is PWM: Fan running



Bracket, VGA, HDMI, DVI	8020055200G
Bracket, VGA, DP(tab), DVI	80200552A0G
Bracket, LP, DP(tab), DVI	8020055300G
Bracket, LP, HDMI, DVI	80200553A0G



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#4B, No. 1367, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Mech/Thermal Management

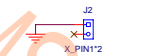
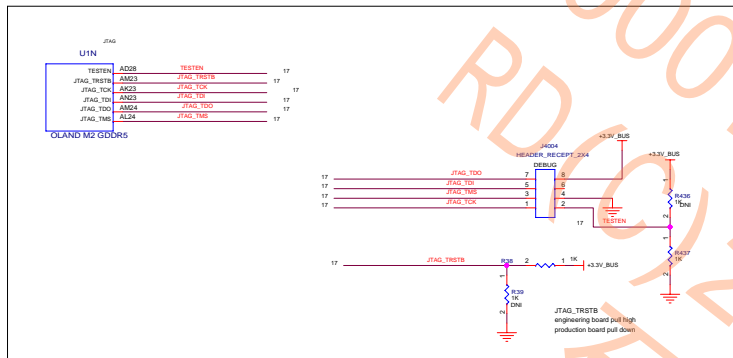
DATE: Mon Sep 21 10:06:42 2015

SHEET NUMBER: 16 OF 20

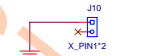
DOCUMENT NUMBER: 105-C8650-008

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TITLE: Oland G5 2GB VGA/sDVI+HDMI/DP



TOP
Single end
RGB
50 ohm +/- 10%
4.02 mils



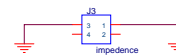
L3_INNER
Single end
Memory data
45 ohm +/- 5 ohm
6.89 mils



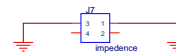
Bottom
Single end
Address trunk
37 ohm +/- 5 ohm
7.05mils



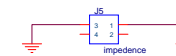
L4_INNER
Single end
Memory data
45 ohm +/- 5 ohm
6.89 mils



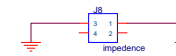
TOP
Different
TMDS
85 ohm +/- 10 %
4.33 mils / 5.511 mils



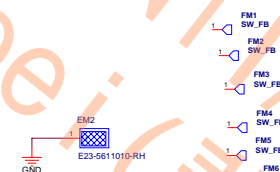
L3_INNER
Different
TMDS
85 ohm +/- 10 %
4.33 mils / 5.511 mils




Bottom
Different
PEX_PCIE
85 ohm +/- 10 %
4.33 mils / 5.51 mils



L4_INNER
Different
Mem Clock
80 ohm +/- 10 %
5.12 mils / 7.48 mils



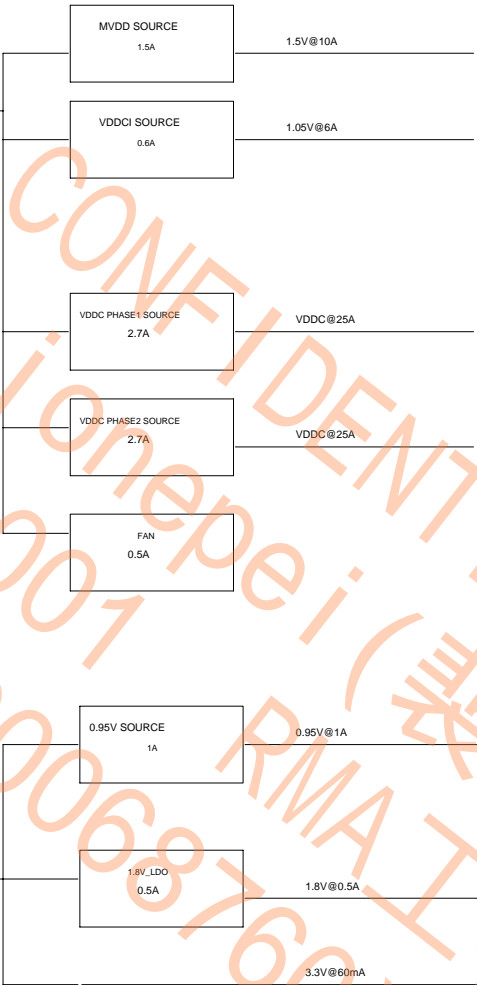
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<p>SHEET: VDDCI</p>	<p>DATE: Tue Sep 22 06:32:59 2015</p>	
<p>SHEET NUMBER: 17</p>	<p>OF 20</p>	<p>REV: 2.0</p>
<p>DOCUMENT NUMBER: 105-C869xx-00B</p>	<p>TITLE:</p> <p style="text-align: center;">Oland G5 2GB VGA/sDVI++HDMI/DP</p>	
<p>NOTES: NOTE</p>		

DW1	HPD4	DDCAUX4
HDM	HPD1	DDCAUX1
DP	HPD3	DDCAUX3

GPIO15	VDDC_VDD	
GPIO20	VDDC_VD1	
GPIO7	VDDC1_VD	DEFAULT1
GPIO5	VIR_HDT	

12V_BUS
5.5A

3.3V_BUS
3A



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SHEET: GPIO DDC HPD map	
DATE: Tue Sep 22 08:32:59 2015	REV: 2.0
SHEET NUMBER: 18 OF 20	
DOCUMENT NUMBER: 105-C869xx-008	
NOTES: NOTE	

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TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP	

8		7		6		5		4		3		2		1	
AMD				TITLE: Oland G5 2GB VGA/sDVI-+HDMI/DP		DOCUMENT NUMBER: 105-C889x-008		DATE: Tue Sep 22 02:20:17 2015		SHEET NUMBER: 20 OF 20		REV: 2.0			
REVISION HISTORY				ENGINEER: Tony Yang		NOTES: NOTE		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of this information included herein.		AMD - PLATFORM HARDWARE ENG #48, No. 1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203					
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
1.00 2.00		000 000		04/19/14 09/22/15		1 Initial release 2 Add VGA, etc									

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石阿鋒 (00068760) RMA工程課